Docket No. 200314976-1

Amendments to the Claims:

Status of Claims:

Claims 1-24 are pending for examination.

Claims 1, 7, 10, 11, 12, and 13 are amended herein.

Claims 1, 12, 13, 14, 22, 23, and 24 are in independent form.

1. (Currently Amended) A system for simulating a processor performance state, comprising:

a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register[[,]] and a set of bit patterns ~~that may be~~ capable of being written to the ACPI throttling register, and

a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns ~~to be written to the ACPI throttling register~~, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register.

2. (Original) The system of claim 1, where the data structure is further configured to store an address of an ACPI status register from which a value related to a throttling status established by the ACPI throttling register can be read.

3. (Original) The system of claim 1, where the memory is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions.

4. (Original) The system of claim 1, where the data structure comprises an ACPI table stored in a memory that is operably connectable to a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions.

5. (Original) The system of claim 1, where the data structure comprises an ACPI table stored in a Basic Input Output System (BIOS) configured to facilitate controlling one or more processor functions.

6. (Original) The system of claim 1, where the set of bit patterns facilitates simulating two processor performance states that correspond to a higher performance state and a lower performance state.

7. (Currently Amended) The system of claim 1, where the processor does not have a variable voltage supply~~set of bit patterns facilitates simulating four processor performance states~~.

8. (Original) The system of claim 1, where the set of bit patterns facilitates simulating two or more processor performance states.

9. (Original) The system of claim 8, where the two or more processor performance states include eight processor performance states simulated by throttling the processor 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time.

10. (Currently Amended) The system of claim 1, where the ACPI throttling register is configured to cause the processor to be throttled by asserting a signal on a STOPCLK# line connected to the processor.

Docket No. 200314976-1

11. (Currently Amended) The system of claim 1, where the processor does not have a variable frequency clock~~10, where the line comprises the STOPCLK# line~~.

12. (Currently Amended) A computer configured with a system for simulating a processor performance state, the system comprising:

a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns capable of being ~~that may be~~ written to the ACPI throttling register, and

a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns ~~to be written to the ACPI throttling register~~, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register.

13. (Currently Amended) A printer configured with a system for simulating a processor performance state, the system comprising:

a data structure stored in a memory, the data structure being configured to store an address of an ACPI throttling register and a set of bit patterns capable of being ~~that may be~~ written to the ACPI throttling register, and

a logic configured to receive a request to establish a desired processor performance state in a processor, to select a bit pattern from the set of bit patterns ~~to be written to the ACPI throttling register~~, and to cause the processor to be throttled in a manner that simulates the desired processor performance state by writing the selected bit pattern to the ACPI throttling register.

14. (Original) A method for simulating a processor performance state, comprising:

receiving a request to establish a processor performance state in a processor;

accessing a data structure to acquire a bit pattern to write to an ACPI throttling register and an address for the ACPI throttling register; and

simulating a processor performance state by causing the processor to be throttled in response to writing the bit pattern to the ACPI throttling register.

15. (Original) The method of claim 14, including establishing the data structure as an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor.

16. (Original) The method of claim 15, where establishing the data structure includes writing a set of bit patterns to the ACPI table and writing the address of the ACPI throttling register to the ACPI table.

17. (Original) The method of claim 14, where the processor performance state corresponds to one of a higher performance state and a lower performance state.

18. (Original) The method of claim 14, where the processor performance state corresponds to one of two or more user defined processor performance states.

19. (Original) The method of claim 14, where the processor performance state corresponds to one of eight processor performance states including a state where the processor is throttled one of 0%, 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, and 87.5% of the time.

20. (Original) The method of claim 14, where writing the bit pattern to the ACPI throttling register causes a signal to be asserted on a STOPCLK# line into the processor.

21. (Original) The method of claim 14, including:

acquiring an address of an ACPI status register configured to report a value related to a throttling status of the processor;

reading the value from the ACPI status register; and

selectively reporting a success or error condition based on the value.

22. (Original) A computer-readable medium storing processor executable instructions operable to perform a method for simulating a processor performance state in a processor, the method comprising:

establishing an ACPI table in a Basic Input Output System (BIOS) operably connectable to the processor, where establishing the ACPI table includes writing a set of bit patterns to the ACPI table, and writing an address of an ACPI throttling register to the ACPI table;

receiving a request to establish a processor performance state in the processor, where the processor performance state corresponds to one of a higher frequency state and a lower frequency state;

accessing the ACPI table to acquire a bit pattern to write to the ACPI throttling register and an address for the ACPI throttling register; and

causing a processor to simulate a processor performance state by throttling the processor by writing the bit pattern to the ACPI throttling register.

23. (Original) A system, comprising:

means for accessing ACPI data;

means for receiving a request to drive a processor into a processor performance state; and

means for controlling a clock signal to the processor by writing data retrieved from the ACPI data to an ACPI throttling register, where controlling the clock signal simulates the processor performance state.

24. (Original) A set of application programming interfaces embodied on a computer-readable medium for execution by a computer component in conjunction with simulating a processor performance state in a processor by controlling an ACPI throttling register, comprising:

a first interface for communicating a bit pattern data;

a second interface for communicating an ACPI throttling register address data; and

a third interface for communicating a state data, where the state data is related to a simulated processor performance state generated by applying the bit pattern data to a register identified by the register address data.